REMARKS

Claims 11-30 are all the claims presently pending in the application.

Applicant gratefully acknowledges that **claims 15-21 are allowed** and that **claim 13 would be allowable** if rewritten in independent form.

Applicant respectfully submits, however, that all of the claims are patentable for the reasons set forth below, and therefore, allowable claim 13 has not been rewritten in independent form at this time. Applicant reserves the right to rewrite allowable claim 13 in independent form at a later time.

New claims 29 and 30 have been added to provide more varied protection for the present invention and should be allowable for somewhat similar reasons as allowable claim 13.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 11, 12, 14, and 22-28 stand rejected on prior art grounds. Particularly, claims 11, 12, and 22-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Uemura et al. (U.S. Patent No. 6,343,334; hereinafter "Uemura") and claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of monitoring a main-clock generated by a main-microcomputer and a sub-clock which is capable of continuing operation in the original state (e.g., using the main-clock) when the main clock is recovered within a specific period of time, or of switching to the sub-clock when the main-clock cannot be recovered within the specific period of time (e.g., see specification at page 3, lines 2-10; see also page 10, lines 17-24 and page 12, lines 18-23).

For example, in an illustrative, non-limiting aspect of the invention, as defined by independent claim 11, a method for monitoring a main-clock generated by a main-microcomputer and a sub-clock, wherein the sub-clock includes a smaller number of clock pulses than those of the main-clock, includes initializing the main-microcomputer at a time point during a specific period of time beginning when it is detected that the main-microcomputer has stopped supply of the main-clock, and when it is confirmed that the main-microcomputer has not resumed supply of the main-clock during the specific period of time, outputting a switch signal to allow switching from the main-clock to the sub-clock.

In another exemplary aspect of the invention, as defined for example by independent claim 22, a method of changing a clock signal from a main-clock supplied by a data processor to a sub-clock includes monitoring the main-clock to detect that the main-clock has stopped, initializing the data processor to attempt to restore the main-clock, and allowing the sub-clock to be supplied instead of the main-clock when the main-clock is not restored during a specific period of time.

Independent claim 23 recites somewhat similar features as those set forth in independent claims 11 and 22.

In conventional methods, when the main clock is stopped for some cause, the stoppage is dealt with by switching the main-clock to the sub-clock. However, when the main-clock is stopped, the main-clock is switched to the sub-clock which continues operating in such a switched state. Thus, a control or the like using software is separately needed to recover the original state (e.g., see specification at page 2, lines 13-26).

The claimed invention, on the other hand, provides a clock monitoring apparatus capable of automatically initializing a main-clock when the main-clock is stopped and continuing operation in a state before abnormality when the main-clock is recovered within a specific period of time, continuing operation by switching the main-clock to a sub-clock when the main-clock cannot be recovered during the specific period of time and issuing a flag when the sub-clock is also stopped to thereby achieve stable operation of a microcomputer even when the main-clock is stopped (e.g., see specification at page 3, lines 2-10; see also page 10, lines 17-24 and page 12, lines 18-23).

II. THE PRIOR ART REJECTIONS

A. Claims 11, 12, and 22-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Uemura. Applicant respectfully disagrees with the Examiner's position, and therefore, traverses this rejection for at least the following reasons.

As defined by independent claims 11, 15, 22, and 23, the main-microcomputer generating **the main-clock is initialized when the main-microcomputer has stopped supply of the main clock**. As a result of initializing the main-microcomputer, the claimed invention is **capable of continuing operating in a state before the main clock stopped when the main clock is**

recovered, and **continuing operation by switching the main clock to the sub clock when the main clock cannot be recovered**.

In contrast, Uemura teaches generating the internal reset signal for resetting the microcomputer 12 **when the external clock 11 is not supplied to the microcomputer 12**. Moreover, the microcomputer 12 is **not** generating the external clock 11. As a result, the internal reset signal does **not** reset a generator for generating the external clock 11.

Therefore, Uemura clearly does **not** disclose or suggest the above mentioned features of the claimed invention, as defined by independent claims 11, 22, and 23, as with allowed claim 15.

Independent claim 11

With respect to independent claim 11, the Examiner alleges that "*the recited "main clock" reads on the external clock 11*" of Uemura, that "*the recited "sub clock" reads on the internal clock signal, i.e., the clock output of ring oscillator 51 (it is disclosed as having a frequency lower than that of clock 11, see column 9, lines 63-67)*", that "*the recited "microcomputer" (or "data processor") of the claims reads on circuitry 12*", and that "*the recited initializing of the microcomputer occurs via the outputting of the internal reset signal from AND gate 30 (see column 4, lines 33-35)*" (see Office Action at pages 2-3, numbered paragraph 4).

The Examiner also alleges that "*the recited "specific time period" reads on the time period starting when it is detected that the external clock 11 has stopped*" and that "*the recited switching over from the stopped external clock 11 to the internal clock occurs in response to the output of Schmitt trigger 43 (this output reads on the recited "switch signal")*" (see Office Action at page 3, numbered paragraph 4).

In addition to the reasons set forth above, Applicant respectfully disagrees with the Examiner's position. That is, Applicant respectfully submits that there are features of the claimed invention which clearly are not disclosed or suggested by the Uemura reference.

For example, independent claim 11 recites, *inter alia*, a method for monitoring a main-clock generated by a main-microcomputer and a sub-clock, including:

> initializing said main-microcomputer at a time point during a specific period of time beginning when it is detected that said main-microcomputer has stopped supply of said main-clock; and
> when it is confirmed that said main-microcomputer has not resumed supply of said main-clock during said specific period of time, outputting a switch signal to allow switching from said main-clock to said sub-clock (emphasis added).

That is, the switch signal is output when it is confirmed that the main-microcomputer has not resumed supply of the main-clock during a specific period of time. In other words, the switch signal is not automatically output when it is detected that the main-microcomputer has stopped supply of the main clock.

As such, the claimed invention is capable of continuing operation in the original state (e.g., using the main-clock) when the main clock is recovered within a specific period of time, or of switching to the sub-clock when the main-clock cannot be recovered within the specific period of time (e.g., see specification at page 3, lines 2-10; see also page 10, lines 17-24 and page 12, lines 18-23).

In comparison (and contrary to the Examiner's position), Uemura does not disclose or suggest that a switch signal is output when it is confirmed that the main-microcomputer has not resumed supply of the main-clock during a specific period of time, as claimed by independent claim 11.

That is, contrary to the Examiner's position set forth above, the recited "*specific time period*" does not "*read on the time period starting when it is detected that the external clock 11 has stopped*" as allegedly disclosed by Uemura. Indeed, Uemura does not disclose, suggest, or even mention a specific period of time as claimed, or basing the switching on a specific period of time and the Examiner has not cited any support in Uemura for this feature.

Instead, as the Examiner points out, Uemura discloses that "*the recited switching over from the stopped external clock 11 to the internal clock occurs in response to the output of Schmitt trigger 43*" (see Office Action at page 3, numbered paragraph 4). Thus, Uemura does not disclose or suggest that the changing over additionally is based on a "*specific period of time*", as claimed.

On the contrary, Uemura discloses only that the switching over from the stopped external clock 11 to the internal clock occurs in response to the output of the Schmitt trigger 43, which results in the clock exchanging circuit 52 exchanging the system clock from the inner clock to the external clock 11 to supply to the micro computer 40.

That is, Uemura specifically discloses that:

> *[T]he Schmitt circuit 43 outputs a signal of "L" to the node D, which implies that the oscillation of the external clock 11 is normal.*
>
> *As a result, the ring oscillator 51 is not actuated, and the clock exchanging circuit 52 continues to supply the external clock 11, as a system clock φ, to the micro computer.*

(see Uemura at column 7, lines 41-46; emphasis added).

On the other hand, Uemura specifically discloses that:

> *[T]he Schmitt circuit 43 outputs a signal of "H" to the node D, which implies that the oscillation of the external clock 11 is stopping.*

> *... thus, the ring oscillator 51 is actuated to oscillate and generates an inner clock signal. Because an oscillation stopping signal of "H" is sent to the clock exchanging circuit 52 from the Schmitt circuit 43, the clock exchanging circuit 52 exchanges the system clock φ from the external clock 11 to the inner clock and supplies it to the micro computer 40.*

(see Uemura at column 7, lines 59-67 and column 8, lines 1-6; emphasis added).

Uemura does not, however, disclose or suggest that a switch signal is output when it is confirmed that the main-microcomputer has not resumed supply of the main-clock during a specific period of time, as claimed.

Instead, as the Examiner acknowledges, Uemura discloses that the clock exchanging circuit 52 switches over from the stopped external clock 11 to the internal clock in response to the output of Schmitt trigger 43 (e.g., see Office Action at page 3, numbered paragraph 4; see also Uemura at column 7, lines 41-46, lines 59-61, and line 67, see also column 8, lines 1-6).

Thus, contrary to the Examiner's position set forth above, the recited "*specific time period*" does not "*read on the time period starting when it is detected that the external clock 11 has stopped*" as allegedly disclosed by Uemura.

Indeed, Uemura does not disclose, suggest, or even mention switching based on a specific period of time, as claimed, and the Examiner has not cited any support in Uemura for this feature.

Should the Examiner maintain that Uemura does teach this feature, Applicant respectfully requests that the Examiner identify such teaching or disclosure in Uemura which switches the external clock to the internal clock based on a specific period of time, as opposed to switching the external clock to the internal clock based on the output of Schmitt trigger 43 (e.g., see Office

Action at page 3, numbered paragraph 4; see also Uemura at column 7, lines 41-46, lines 59-61, and line 67, see also column 8, lines 1-6).

For the foregoing reasons, Applicant respectfully submits that Uemura clearly does not disclose or suggest confirming that the main-clock has not resumed supply of the main-clock during a specific period of time, and then outputting a switch signal to allow switching from the main-clock to the sub-clock, as claimed by independent claim 11.

Moreover, as mentioned above, the main-microcomputer generating **the main-clock is initialized when the main-microcomputer has stopped supply of the main clock**. As a result of initializing the main-microcomputer, the claimed invention is **capable of continuing operating in a state before the main clock stopped when the main clock is recovered**, and **continuing operation by switching the main clock to the sub clock when the main clock cannot be recovered**.

In contrast, Uemura teaches generating the internal reset signal for resetting the microcomputer 12 **when the external clock 11 is not supplied to the microcomputer 12**. Further, the microcomputer 12 is **not** generating the external clock 11. As a result, the internal reset signal does **not** reset a generator for generating the external clock 11.

Therefore, Uemura clearly does **not** disclose or suggest the above mentioned features of the claimed invention, as defined by independent claim 11.

Accordingly, Applicant submits that independent claim 11 clearly is not anticipated by Uemura.

Dependent Claims 12 and 24-28

Moreover, in addition to the reasons set forth above with respect to the independent claims, Applicant submits that dependent claims 12 and 24-28 also are not anticipated by

Uemura based on their dependency from claim 11, as well as for the additional features recited therein.

For example, with respect to dependent claim 24, the Examiner alleges that column 8, lines 44-55 of Uemura discloses this feature.

However, contrary to the Examiner's position, Applicant respectfully submits that Uemura does not disclose or suggest this feature of the invention, as defined by dependent claim 24.

That is, Uemura does not disclose or suggest that "*when it is confirmed that said main-microcomputer has resumed supply of said main-clock during said specific period of time, determining that said main-microcomputer has been restored to normal operations*" (emphasis added).

As with independent claim 11, Uemura does not disclose or suggest that the switching from the inner clock to the external clock, or for that matter, determining whether the external clock has been restored to normal operation based on a "*specific period of time*", as claimed by dependent claim 24.

For example, Uemura specifically discloses that:

> *After an oscillation stopping period, in which the oscillation of the external clock stops and the system clock is exchanged to the inner clock, as shown in FIG. 5, if the external clock 11 begins to oscillate again, while the detection of oscillation stopping is allowed, one shot pulse of "H" appears at every standing up and standing down edge of the external clock 11 at the node B. The voltage of the node C is sawtooth wave form and does not exceed the predetermined threshold voltage of the Schmitt circuit 43. Therefore the Schmidt circuit 43 outputs a signal of "L" to the node D, which implies that the oscillation of the external clock 11 is normal.*
>
> *As a result, ... [a]n oscillation stopping signal of "L" is input to the clock exchanging circuit 52, therefore the clock exchanging circuit 52*

> *exchanges the system clock φ from the inner clock to the external clock 11 to supply to the micro computer 40.*

(see Uemura at column 8, lines 44-64; emphasis Applicants).

In comparison, dependent claim 24 recites, *inter alia*, that "*when it is confirmed that said main-microcomputer has resumed supply of said main-clock during said specific period of time, determining that said main-microcomputer has been restored to normal operations*" (emphasis added).

On the other hand, in the claimed invention, if the main clock resumes or recovers within the specific period of time, then the switch signal would not be output, as defined by dependent claim 26.

That is, dependent claim 26 recites, *inter alia*, "*when it is confirmed that said main-microcomputer has resumed supply of said main-clock during said specific period of time, determining that outputting a switch signal to switch from said main-clock to said sub-clock is not necessary*" (emphasis added).

In comparison, and as the Examiner points out, Uemura merely discloses that after the external clock stops and the system clock is exchanged to the inner clock, as shown in Figure 5, if the external clock 11 begins to oscillate again, the Schmidt circuit 43 outputs a signal of "L" to the node D, which implies that the oscillation of the external clock 11 is normal, and as a result, the clock exchanging circuit 52 exchanges the system clock φ from the inner clock to the external clock 11 to supply to the micro computer 40 (e.g., see Uemura at column 8, lines 44-64).

In other words, Uemura clearly discloses that the system clock is already exchanged to the inner clock before the alleged determination is made as to whether the external clock 11 begins to oscillate again.

Uemura switches to the inner clock regardless of whether the main clock recovers within a specific period of time, as claimed. Only after the switch from the external clock 11 to the inner clock has been made, does Uemura disclose switching from the inner clock back to the external clock 11, as specifically disclosed by Uemura (see Uemura at column 8, lines 44-64).

This is completely different from the claimed invention which waits a specific period of time to determine if switching from the main clock to the sub-clock is even necessary. If the main-clock is restored (resumed) during the specific period of time, no switching is required (i.e., necessary), as claimed by claim 26 (e.g., see specification at page 3, lines 2-10; see also page 10, lines 17-24 and page 12, lines 18-23).

Thus, Uemura clearly does not disclose or suggest that "*when it is confirmed that said main-microcomputer has resumed supply of said main-clock during said specific period of time, determining that outputting a switch signal to switch from said main-clock to said sub-clock is not necessary*" as recited by dependent claim 26.

Independent Claim 22

Independent claim 22 recites, *inter alia*,

> a method of changing a clock signal from a main-clock supplied by a data processor to a sub-clock, comprising:
> monitoring said main-clock to detect that said main-clock has stopped;
> initializing said data processor to attempt to restore said main-clock; and
> allowing said sub-clock to be supplied instead of said main-clock when said main-clock is not restored during a specific period of time (emphasis added).

As mentioned above, the main-microcomputer generating **the main-clock is initialized when the main-microcomputer has stopped supply of the main clock**. As a result of initializing the main-microcomputer, the claimed invention is **capable of continuing operating**

in a state before the main clock stopped when the main clock is recovered, and **continuing operation by switching the main clock to the sub clock when the main clock cannot be recovered**.

In contrast, Uemura teaches generating the internal reset signal for resetting the microcomputer 12 **when the external clock 11 is not supplied to the microcomputer 12**. Moreover, the microcomputer 12 is **not** generating the external clock 11. As a result, the internal reset signal does **not** reset a generator for generating the external clock 11. Therefore, Uemura clearly does **not** disclose or suggest the above mentioned features of the claimed invention, as defined by independent claim 22.

Also, Uemura clearly does not disclose or suggest allowing the sub-clock to be supplied instead of the main-clock when the main-clock is not restored during a specific period of time, as claimed.

Instead, Uemura switches to the sub-clock regardless of whether the main-clock recovers within a specific period of time, as claimed. This is completely different from the claimed invention which waits a specific period of time to determine if switching to the sub-clock is even necessary.

Thus, for somewhat similar reasons as those set forth above with respect to claim 11, Applicant submits that Uemura clearly does not disclose or suggest all of the features of independent claim 22. Therefore, the rejection of claim 22 also should be withdrawn.

Independent Claim 23

Independent claim 23 recites, *inter alia*, a method for monitoring a main-clock generated by a main-microcomputer and a sub-clock, the method including:

> detecting whether said main-microcomputer has stopped supply of said main-clock;
> initializing said main-microcomputer at a time point during a specific period of time beginning when said detecting detects that said main-microcomputer has stopped supply of said main-clock;
> confirming whether said main-microcomputer has resumed supply of said main-clock during said specific period of time; and
> outputting a switch signal to switch from said main-clock to said sub-clock when said confirming confirms that said main-microcomputer has not resumed supply of said main-clock during said specific period of time,
> wherein a number of clock pulses of said sub-clock is less than a number of clock pulses of said main-clock (emphasis added).

As mentioned above, Uemura clearly does not disclose or suggest allowing the sub-clock to be supplied instead of the main-clock when the main-clock is not restored during a specific period of time, as claimed.

Instead, Uemura switches to the sub-clock regardless of whether the main-clock recovers within a specific period of time, as claimed. This is completely different from the claimed invention which waits a specific period of time to determine if switching to the sub-clock is even necessary.

As mentioned above, the main-microcomputer generating **the main-clock is initialized when the main-microcomputer has stopped supply of the main clock**. As a result of initializing the main-microcomputer, the claimed invention is **capable of continuing operating in a state before the main clock stopped when the main clock is recovered**, and **continuing operation by switching the main clock to the sub clock when the main clock cannot be recovered**.

In contrast, Uemura teaches generating the internal reset signal for resetting the microcomputer 12 **when the external clock 11 is not supplied to the microcomputer 12**.

Moreover, the microcomputer 12 is **not** generating the external clock 11. As a result, the internal reset signal does **not** reset a generator for generating the external clock 11. Therefore, Uemura clearly does **not** disclose or suggest the above mentioned features of the claimed invention, as defined by independent claim 23.

Thus, for somewhat similar reasons as those set forth above with respect to claim 11, Applicant submits that Uemura clearly does not disclose or suggest all of the features of independent claim 23. Therefore, the rejection of claim 23 also should be withdrawn.

B. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Uemura.

However, Applicant respectfully submits that claim 14 is patentable over Uemura at least by virtue of its dependency from independent claim 11. Therefore, Applicant respectfully requests that the Examiner withdraw this rejection.

III. NEW CLAIMS

New claims 29 and 30 are added to provide more varied protection for the present invention.

Applicant submits that claims 29 and 30 define somewhat similar features as allowable claim 13. Thus, Applicant submits that claims 29 and 30 are patentable for somewhat similar reasons as allowable claim 13, and therefore, respectfully requests allowance of claims 29 and 30.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 11-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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John J. Dresch, Esq.
Registration No. 46,672

Sean M. McGinn
Registration No. 34,386

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254